

WHAT IS CLAIMED IS:

1 1. A reconfigurable bit-manipulation node, comprising:
2 an execution unit configured to perform a plurality of bit-oriented functions;
3 and
4 a control unit configured to control the execution unit to allow one of the
5 plurality of bit-oriented functions to be performed;
6 wherein the execution unit includes a plurality of elements interconnected with
7 one another to allow the plurality of bit-oriented functions to be performed, the plurality of
8 elements including a programmable butterfly unit, a plurality of non-programmable butterfly
9 units, a plurality of data path elements, a look-up-table memory and a reorder memory; and
10 wherein the execution unit is capable of engaging in one of a plurality of
11 operating modes to perform the plurality of bit-oriented functions, the plurality of operating
12 modes including a programmable mode and a plurality of fixed operating modes.

1 2. The node of claim 1 wherein the plurality of fixed operating modes
2 include a Viterbi mode, a turbo decoder soft-in-soft-out mode, a variable length encoding
3 mode and a variable decoding mode.

1 3. The node of claim 1 wherein when engaged in the programmable
2 mode, the execution unit does not utilize the plurality of non-programmable butterfly units.

1 4. The node of claim 2 wherein when engaged in the Viterbi mode, the
2 execution unit utilizes both the programmable butterfly unit and the plurality of non-
3 programmable butterfly units and uses the look-up-table memory as a path metric memory
4 and the reorder memory as a trace back memory.

1 5. The node of claim 2 wherein when engaged in the turbo decoder soft-
2 in-soft-out mode, the execution unit utilizes both the programmable butterfly unit and three of
3 the plurality of non-programmable butterfly units.

1 6. The node of claim 2 wherein when engaged in the variable length
2 encoding mode or the variable length decoding mode, the execution unit only uses a subset of
3 a plurality of operations available from the programmable butterfly unit.

- 1 7. The node of claim 1 wherein one or more of the plurality of bit-
2 oriented functions are fixed.
- 1 8. The node of claim 7 wherein the one or more of the plurality of bit-
2 oriented functions that are fixed include Viterbi decoding, turbo decoding and variable length
3 encoding and decoding.
- 1 9. The node of claim 1 wherein one or more of the plurality of bit-
2 oriented functions are programmable.
- 1 10. The node of claim 9 wherein the one or more of the plurality of bit-
2 oriented functions that are programmable include scrambling, cyclical redundancy check and
3 convolutional encoding.
- 1 11. The node of claim 1 wherein the plurality of bit-oriented functions are
2 used to handle a plurality of channel coding schemes.
- 1 12. The node of claim 11 wherein the plurality of channel schemes include
2 error detecting cyclic codes, error detecting and correcting Hamming codes and single burst
3 error correcting Fire codes.
- 1 13. The node of claim 1 wherein the control unit controls the execution
2 unit by using a plurality of control bits including fixed control bits, counter control bits and
3 state control bits.
- 1 14. The node of claim 1 wherein the plurality of data path elements include
2 a shifter having a plurality of inputs.
- 1 15. The node of claim 14 wherein the shifter is programmable on a cycle-
2 by-cycle basis and configured to perform an exclusive-or (XOR) function on multiple shifted
3 versions of the plurality of inputs.
- 1 16. The node of claim 15 wherein the shifter is further programmable to
2 implement a parallel linear feedback shift register.
- 1 17. The node of claim 16 wherein the parallel linear feedback shifter
2 register includes a parallel maskable linear feedback shifter.

1 18. The node of claim 1 wherein the plurality of data path elements include
2 a programmable data combiner.

1 19. The node of claim 18 wherein the combiner is configured to perform
2 packing on an input to generate an output word, the input capable of having one of a plurality
3 of input lengths including 1-bit length, 4-bit length, 8-bit length, 16-bit length and 32-bit
4 length, the output word capable of having one of a plurality of output lengths including 8-bit
5 length, 16-bit length and 32-bit length.

1 20. The node of claim 19 wherein the combiner is further configured to
2 perform bit interlacing.

1 21. The node of claim 20 wherein the combiner is further configured to
2 perform packing and bit interlacing simultaneously.

1 22. The node of claim 20 wherein the combiner is further configured to
2 perform bit puncturing.

1 23. The node of claim 22 wherein the combiner is further configured to
2 perform packing, bit interlacing and bit puncturing simultaneously.

1 24. The node of claim 1 wherein the plurality of data path elements include
2 an unpacker, the unpacker configured to perform unpacking on an input word to generate an
3 output, the input word capable of having one of a plurality of input lengths including 16-bit
4 length and 32-bit length, the output capable of having one of a plurality of output lengths
5 including 4-bit length, 8-bit length and 16-bit length.

1 25. The node of claim 24 wherein the unpacker is further configured to
2 perform sign extension.

1 26. A programmable shifter comprising:
2 circuit configured to receive a plurality of inputs; and
3 circuit configured to perform an exclusive-or (XOR) function on multiple
4 shifted versions of the plurality of inputs;
5 wherein the shifter is programmable on a cycle-by-cycle basis.

- 1 27. The shifter of claim 26 wherein the shifter is programmable to
2 implement a parallel linear feedback shift register.
- 1 28. The shifter of claim 27 wherein the parallel linear feedback shifter
2 register includes a parallel maskable linear feedback shifter register.
- 1 29. A reconfigurable bit-manipulation node utilizing the shifter as recited
2 in claim 26.
- 1 30. A programmable data combiner comprising:
2 circuit configured to receive an input, the input capable of having one of a
3 plurality of input lengths including 1-bit length, 4-bit length, 8-bit length, 16-bit length and
4 32-bit length,; and
5 circuit configured to perform packing on the input to generate an output word,
6 the output word capable of having one of a plurality of output lengths including 8-bit length,
7 16-bit length and 32-bit length.
- 1 31. The combiner of claim 30 further comprising:
2 circuit configured to perform bit interlacing.
- 1 32. The combiner of claim 31 wherein the combiner performs packing and
2 bit interlacing simultaneously.
- 1 33. The combiner of claim 31 further comprising:
2 circuit configured to perform bit puncturing.
- 1 34. The combiner of claim 33 wherein the combiner performs packing, bit
2 interlacing and bit puncturing simultaneously.
- 1 35. A reconfigurable bit-manipulation node utilizing the programmable
2 data combiner as recited in claim 30.